

**TRANSMITTAL LETTER
(General - Patent Pending)**

Docket No.
SEC.1067

In Re Application Of: **Myun-Joo PARK et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/644,735	August 21, 2003	Trong Q. Phan	20987	2827	6201

Title: **SEMICONDUCTOR MEMORY SYSTEM HAVING MULTIPLE SYSTEM DATA BUSES**

COMMISSIONER FOR PATENTS:

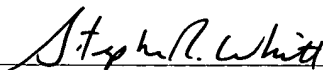
Transmitted herewith is:

Request for Reconsideration

in the above identified application.

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Signature

Dated: **September 16, 2005**

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Application No. 10/644,735
SEC.1067

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of :
Inventor: Myun-Joo PARK et al. : Group Art Unit: 2827
Application No. 10/644,735 : Examiner: PHAN, Trong Q
Filing Date: August 21, 2003 :
Title: SEMICONDUCTOR MEMORY SYSTEM HAVING MULTIPLE
SYSTEM DATA BUSES

REQUEST FOR RECONSIDERATION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In the Office Action dated June 24, 2005, claims 1-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,414,904 to So et al. (hereafter, So). The rejection is respectfully traversed for at least the following reasons.

According to the Office Action, Fig. 1 of So shows a “memory controller”, eight (8) “system data buses DB1 to DB8”, four (4) “memory modules 12a to 12d”, and a “common control and address bus CAB” (See, Office Action at paragraph 2, lines 3-9).

Unfortunately, the Office Action completely ignores the fact that independent claims 1, 8, and 15 each recite “N system data buses” having a specific correspondence with “N memory modules”. For example, claim 1 recites that each of the “N memory modules...are connected to a respectively *different one* of the N system data buses” (emphasis added). The Office Action

further ignores the fact that independent claims 1 and 15 each recite “first through P-th memory module groups”, each “having N memory modules” (See, claims 1 and 15).

In Fig. 1 of So, four (4) of the so called “system data buses” (DB1 through DB4) are connected to two (2) of the memory modules 12a and 12b, and four (4) more of the system data buses (DB5 through DB8) are connected to two (2) more of the memory modules 12c and 12d. Memory modules 12a and 12b are referred to as a “first group” and memory modules 12c and 12d are referred to as a “second group” (See, So at col. 3, lines 43-47). Accordingly, Fig. 1 in So shows two (2) groups, each having two (2) memory modules, where the memory modules in each of the two groups are connected to a separate and distinct set of “system data buses”.

Given these indisputable facts, So fails to support any rejection of independent claim 1 under 35 U.S.C. § 103 on at least two counts. First, each one of the memory modules within a group is connected to exactly the same system data buses, i.e., the memory modules in the first group are all connected to data buses DB1 through DB4, and the memory modules in the second group are all connected to data buses DB5 through DB8. Thus, the memory modules “within each of the...module groups” in the So system are not “connected to a respectively *different* one of the N system data buses” as recited in claim 1. (Emphasis added).

Second, So fails to disclose “N system data buses” and memory module groups having “N memory modules” as recited by claim 1. To illustrate, suppose that the number “N” of system data buses is 2. Now, select any two of the data buses (DB1 through DB8) in Fig. 1 of So. One will notice that the two selected data buses are not connected with memory modules 12a to 12d such that both modules in the first and second groups are connected to different system data buses. The same would be true for any subset of size $N \geq 2$ of data

buses DB1 to DB8. Accordingly, the disclosure of So relative to Fig. 1 does not anticipate or render obvious claim 1 of the subject application.

Similarly, the stated rejection of independent claim 8 is unsupported for at least the following reasons. First, So fails to disclose “a first memory module group having N memory modules respectively connected to the N system data buses” as recited in claim 8, because the number of memory modules disclosed in So is different from the number of modules in each memory module group. Second, So fails to disclose “a second memory module group having at least one memory module connected to *all* of the N system data buses” as recited in claim 8. Instead, each of the memory modules in So is connected to only half of the data buses DB1 to DB8.

Similarly, the stated rejection of claim 15 is unsupported by So for at least the following reasons. First, So fails to disclose “N system data buses” and memory module groups having “N memory modules” as recited by claim 15. Second, So fails to disclose data buffers connected to each of the memory modules. Third, So fails to disclose that the memory modules are connected to “different ones of the N system data buses” as recited by claim 15.

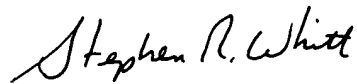
The noted differences between the specific claim language and the disclosure presented in So are material and can not simply be swept aside as some unsubstantiated “obvious” variations. If So is deemed to suggest the *claimed invention* some explanation as to how or why the very different structure presented in So obviates the pending claims must be forthcoming, so that the applicants may address the obvious conclusion on the merits, or amend the pending claims, if appropriate.

Because So (or any reasonable combination of So with the art of record) fails to teach or suggest all the claim limitations recited in independent claims 1, 8, and 15, the rejection of the pending independent claims under 35 U.S.C. § 103 is unwarranted and should be withdrawn. For at least the foregoing

reasons, the rejection of dependent claims 2-7, 9-14, and 16-21 is also unwarranted and should also be withdrawn.

No other issues remaining, reconsideration and favorable action on claims 1-21 is requested.

Respectfully submitted,



Date: September 16, 2005

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